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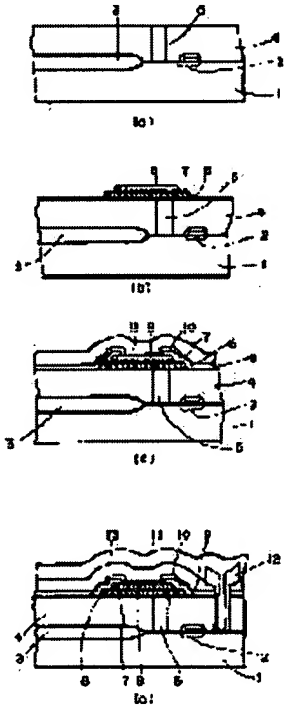
## (54) MANUFACTURE OF SEMICONDUCTOR STORAGE ELEMENT

(57)Abstract:

PROBLEM TO BE SOLVED: To see to it that stable transistor properties can be obtained, with an interface state density of a gate oxide film reduced by terminating the defects at the interface between the gate oxide film of a switching transistor and a silicon substrate by hydrogen, without having the ferroelectric properties deteriorated.

SOLUTION: The detects at an interface between the gate insulating film of a MOS transistor and a silicon substrate 1 are terminated by heat-treating them in hydrogen atmosphere or a mixed atmosphere of hydrogen and inert gas after forming a ferroelectric film 8 on a lower electrode 7, and crystallizing the ferroelectric film 8. Next, an upper electrode 10 is made on the ferroelectric film 8 via the contact hole made in a second interlayer insulating film 9. Next, after the formation of a third inter-layer insulating film 1, a contact hole is made, and metal wiring 12 for connecting the MOS transistor 2 with other semiconductor storage element is made, and then a surface protective film 13 is made on the surface.



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## DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the manufacture approach of a semi-conductor storage element, and the manufacture approach of the semi-conductor storage element equipped with the capacitor which makes a ferroelectric a dielectric film in more detail.
[0002]
[Description of the Prior Art] The nonvolatile memory using the conventional ferroelectric is shown in drawing 1 . The conventional ferroelectric random-access memory is constituted by at least one switching transistor and at least one ferroelectric capacitor. After forming a switching transistor in the active region surrounded by isolation like the CMOS process of the conventional DRAM, a ferroelectric is formed after the lower electrode formation equivalent to a drive line on a component isolation region. As for stored charge, a ferroelectric capacitor shows a hysteresis property to impression electric field.
[0003] Even if it removes impression electric field, since the ferroelectric film has spontaneous polarization, information (1 or 0) is memorized by this direction of polarization. By using this property, even if it turns off the power, the nonvolatile memory which can hold information is realizable. The threshold electrical potential difference of the positive/negative for carrying out polarization reversal, for applying to memory is equal, and in order for the sensing amplifier of semiconductor memory to detect the difference of the amount of reversal charges, and the amount of noninverting charges, it is needed about two 5microC/cm.
[0004] Moreover, an up plate electrode, the PZT film, and a drive line are simultaneously processed into a predetermined configuration after ferroelectric capacitor formation. It has the structure where the plate electrode of a bit line, and the source / drain field of another side, and a ferroelectric capacitor was electrically connected to one source / drain field by wiring.
[0005] Titanic-acid lead zirconate (referred to as "PZT" PbZrxTi1-xO3 and the following.) or a bismuth stratified compound (SrBi4Ti 4O15, SrBi2Ta 2O9) is used for the ferroelectric ingredient as an ingredient with which are satisfied of the above-mentioned property. Moreover, the junction nature of a grid with the PZT film is good for an electrode material, and RuO2, IrO2, LaSrCoO, etc. which are oxidation-resistant outstanding PtRh and outstanding PtRhOx, and an oxidation-resistant oxide, and have the description of conductivity are used for it. An interlayer insulation film is formed after forming a ferroelectric capacitor, and between components is connected using metal wiring. The oxidation silicon film or a silicon nitride film is formed in an interlayer insulation film with a CVD method, using silane gas or TEOS (tetra-ethoxy silane) as a raw material.
[0006] Thus, the memory equipped with the transistor heat-treats within the limits of 400-450 degrees C in the inert gas ambient atmosphere which usually contains hydrogen after final process completion like metal wiring or protective coat formation. This is for reducing the interface-state-density consistency of gate oxide, and acquiring stable transistor characteristics by carrying out termination to the gate oxide of a transistor, and a substrate from the hydrogen which diffused the defect of an interface.
[0007] Hereafter, the technique indicated by JP,7-273297,A as a conventional technique is explained

using drawing 3 .
[0008] First, after forming the component isolation region 42 in semi-conductor substrate 41 front face, the switching transistor 47 which has the gate electrode 46 formed through gate dielectric film 45 on the source 43, and the diffusion field of a drain 44 and a substrate 41 is formed.
[0009] Next, the BPSG film 48 is formed as an interlayer insulation film, and sequential formation of the titanium glue line 49 of 20nm of thickness, the Pt lower electrode 51 whose thickness is 200nm, the ferroelectric thin film 52 which is 250nm of thickness, and the Pt up electrode 53 which is 200nm of thickness is further carried out on the BPSG film 48.
[0010] Next, the 2nd protective coat 55 of 220nm of thickness which the 1st protective coat 54 of the silicon oxide of 200nm of thickness which consists of SOG formed, and was further formed on the 1st protective coat 54 by spreading heat treatment of the MOD solution of the same presentation as the construction material of the ferroelectric thin film 52 is formed. Baking of the 2nd protective coat 55 is the same as the processing conditions of the ferroelectric thin film 52.
[0011] Furthermore, on the 2nd protective coat 55, the interlayer insulation film 56 of 300nm of thickness by the silane pyrolysis by LPCVD membrane formation is formed. Opening 57 is formed in the 1st protective coat 54 corresponding to the source 43 and a drain 44, the 2nd protective coat 55, the interlayer insulation film 56, and the BPSG film 48 of this switching transistor 47, and the source ejection wiring 58 and the drain ejection wiring 59 are formed in this opening 57. Moreover, opening 57 is formed also in the 1st protective coat 54 corresponding to the up electrode 53 and the lower electrode 51, the 2nd protective coat 55, and an interlayer insulation film 56, and the up electrode ejection wiring 59 and the up electrode ejection wiring 60 are electrically connected to these openings 57.
[0012] The interlayer insulation film used among multilayer interconnections, such as aluminum, or the protective coat formed after the completion of wiring needs to carry out substrate temperature at the time of formation before and after 400 degrees C after capacitor formation in consideration of the reaction of aluminum wiring and a silicon substrate, and the dependability of aluminum wiring. For this reason, conventionally, a silane and TEOS are used as a raw material and the interlayer insulation film and the protective coat are formed by the plasma-CVD method which can be formed at low temperature.
[0013] However, a lot of hydrogen is contained in the interlayer insulation film formed by silane gas or the plasma CVD method using TEOS, this hydrogen is dissociated by heat treatment around 400 degrees C after protective coat formation, if it activates with the up Pt electrode of diffusion and a ferroelectric capacitor and a ferroelectric film interface is reached, a reduction operation will generate the interior of a component in a ferroelectric film side, the oxygen in the film is drawn out, and insulation is destroyed. If this phenomenon progresses, a ferroelectric property will deteriorate and leakage current will increase. Moreover, in order to heat-treat in the inert gas ambient atmosphere which contains hydrogen after up electrode formation, degradation of a ferroelectric property and the increment in leakage current take place similarly.
[0014] Moreover, when using the thin film 55 equal to a ferroelectric also in crystal structure also in presentation as a protective coat of hydrogen cutoff nature, flattening of this protective coat is difficult, and peeling by the insulator layer on a protective coat occurs, or the element which constitutes a protective coat is spread and it has problems, such as having an adverse effect on a switching transistor etc.
[0015]
[Means for Solving the Problem] The manufacture approach of the semi-conductor storage element of this invention according to claim 1 The MOS transistor used as the switching transistor formed in the semi-conductor substrate, Connect with the above-mentioned MOS transistor and an electric target through the contact hole formed in the 1st interlayer insulation film, have the capacitor which makes the ferroelectric film a dielectric film, and wiring is minded. In the manufacture approach of the semi-conductor storage element connected with other semi-conductor storage elements By carrying out 1st heat treatment in the mixed ambient atmosphere of hydrogen or hydrogen, and inert gas, after crystallizing the above-mentioned ferroelectric film, the process which forms the above-mentioned ferroelectric film on the lower electrode of the above-mentioned capacitor, and The process which

carries out termination of the defect in the interface of the gate dielectric film of the above-mentioned MOS transistor, and the above-mentioned semi-conductor substrate, The process which forms the up electrode of the above-mentioned capacitor through the contact hole formed in direct or the 2nd interlayer insulation film on the above-mentioned ferroelectric film, After forming the 3rd interlayer insulation film, it is characterized by forming a contact hole, forming wiring which connects the above-mentioned MOS transistor and other semi-conductor storage elements, and forming a surface protective coat in a front face after that.

[0016] Moreover, the manufacture approach of the semi-conductor storage element of this invention according to claim 2 is the manufacture approach of the semi-conductor storage element according to claim 1 characterized by performing the 1st above-mentioned heat treatment at 300-450 degrees C.

[0017] Moreover, the manufacture approach of the semi-conductor storage element of this invention according to claim 3 is the manufacture approach of the semi-conductor storage element according to claim 1 or 2 characterized by forming the oxidation silicon film, silicon nitride film, or nitriding oxidation silicon film containing a fluorine by the chemical vapor deposition which used silicon tetrafluoride as a raw material as the 1st interlayer insulation film of the above, the 2nd interlayer insulation film of the above, the 3rd interlayer insulation film of the above, and the above-mentioned surface protective coat.

[0018] Moreover, the manufacture approach of the semi-conductor storage element of this invention according to claim 4 is the manufacture approach of the semi-conductor storage element according to claim 1 to 3 characterized by carrying out 2nd heat treatment in the mixed-gas ambient atmosphere of oxygen, inert gas, or oxygen and inert gas, after forming the above-mentioned surface protective coat.

[0019] Furthermore, the manufacture approach of the semi-conductor storage element of this invention according to claim 5 is the manufacture approach of the semi-conductor storage element according to claim 1 to 4 characterized by performing the 2nd above-mentioned heat treatment at 300-450 degrees C.

[0020]

[Embodiment of the Invention] Hereafter, this invention is explained to a detail based on the gestalt of operation.

[0021] drawing 1 -- production process drawing of the semi-conductor storage element of the gestalt of 1 operation of this invention -- it is -- 1 -- a semi-conductor substrate and 2 -- a switching transistor and 3 -- a component isolation region and 4 -- the 1st interlayer insulation film and 5 -- a polish recon plug and 6 -- a barrier metal layer and 7 -- the lower electrode of a capacitor, and 8 -- in the ferroelectric film and 9, the 3rd interlayer insulation film and 12 show metal wiring, and, as for the 2nd interlayer insulation film and 10, 13 shows a surface protective coat, as for an up electrode and 11.

[0022] Hereafter, the production process of the semi-conductor storage element of the gestalt of 1 operation of this invention is explained.

[0023] First, according to the well-known transistor manufacture approach, the MOS transistor and component isolation region used as a switching transistor 2 are formed on a silicon substrate 1. The SiOF film which used the BPSG film (boron phosphorus dope silicon oxide) or silicon tetrafluoride (SiF4) for the raw material is formed as the 1st interlayer insulation film 4 on a silicon substrate 1.

[0024] Next, the resist pattern formation back for contact hole formation is carried out according to a lithography process, and opening of the KONTOKUTO hole is carried out by the dry etching method. Next, the polish recon film is deposited and phosphorus is doped in a 800-900-degree C ambient atmosphere. Next, the polish recon film is ground by chemical mechanical polish, and the polish recon plug 5 is formed in a contact hole. Next, Ti film (not shown) of 200A of thickness is formed as an adhesion layer with the 7/barrier metal layer 6 of lower electrodes.

[0025] Next, the 1000-2000A titanium nitride film, TaSiN film, or these cascade screens are formed depending on the method of sputtering as a barrier metal layer 6 of the lower electrode 7 and the polish recon plug 5. In addition, in the gestalt of this operation, the TiN film is used as a barrier metal layer 6. Next, oxide electrodes or these cascade screens, such as the compound which contains Pt of 500-1500A of thickness or Pt as a lower electrode 7, or IrO2, RuO2, ReO3, are formed by the sputtering method. In addition, Pt film is used in the gestalt of this operation.

[0026] next, the lower electrode 7 top -- the sol-gel method -- the PZT film of 2000A of thickness -- forming -- lamp **** -- the perovskite structure which has a ferroelectricity by a certain ******** is crystallized, and the ferroelectric film 8 is formed. Although crystallization temperature changes greatly with ferroelectric ingredients, by the PZT film or the PLZT film, 600-700 degrees C is desirable.
[0027] Next, patterning of the PZT film, and the lower electrode Pt/TiN film / Ti film is carried out. It processes in a 300-450-degree C temperature requirement in the inert gas ambient atmosphere which contains hydrogen or hydrogen after patterning. Thereby, termination of Si substrate, the gate oxide of a switching transistor, and the defect of an interface is carried out by hydrogen.
[0028] Thus, by carrying out heat treatment in the inert gas containing hydrogen, before forming an up electrode, as shown in drawing 2 (a), degradation is not seen by the ferroelectric property. On the other hand, when it processes in the inert gas which contains hydrogen after up electrode formation, as shown in drawing 2 (b), degradation of a ferroelectric property is remarkable.
[0029] If it heat-treats in the ambient atmosphere which contains hydrogen after up electrode formation from this, occlusion of the hydrogen will be easily carried out to an up electrode, and it will be considered to reach a ferroelectric interface. And it has the catalysis, hydrogen is activated, a reduction operation occurs in a ferroelectric film side, and an up electrode, especially Pt are considered that the oxygen in the film is drawn out. If this phenomenon progresses, a ferroelectric property will deteriorate and leakage current will increase. From this, when heat-treating in a hydrogen ambient atmosphere, it is necessary to carry out before capacitor up electrode formation.
[0030] Next, the 2nd interlayer insulation film 9 is formed on the PZT film. In the 2nd interlayer insulation film 9, by the plasma-CVD method, SiF4, and O2 and Ar are used as a raw material, substrate temperature uses SiF4, N2, O2 and Ar, or N2O as a raw material in an ordinary temperature -450 degree C temperature requirement, and substrate temperature forms the SiONF film in an ordinary temperature -450 degree C temperature requirement. [ the SiOF film, ] Since the film formed by the above-mentioned approach does not use hydrogen content gas for membrane formation gas, hydrogen (H) does not exist in the film.
[0031] Next, opening of the contact hole for up electrode 10 formation is carried out. As an up electrode 10, about 1000A of Pt(s) is formed and patterning is carried out according to a photolithography process. The up electrode 10 is not limited to Pt and may use the oxide conductors used with the lower electrode 7, or these laminating electrodes.
[0032] Next, on the up electrode 10, the 3rd interlayer insulation film 11 is used and the same approach as the 2nd interlayer insulation film 9 is formed. Next, on the source of a switching transistor 2, opening of the contact hole is carried out and the metal wiring 12 is formed.
[0033] after metal wiring 12 formation and as the surface protective coat 13 -- SiF4, and O2 and Ar -- a raw material -- carrying out -- substrate temperature -- the inside of an ordinary temperature -450 degree C temperature requirement -- the SiOF film -- or SiF4, and N2 and Ar are used as a raw material. Substrate temperature in an ordinary temperature -450 degree C temperature requirement The SiNF film, SiF4, N2, O2 and Ar, or N2O is used as a raw material. Substrate temperature in an ordinary temperature -450 degree C temperature requirement Or the SiONF film, The silicon nitride film by the plasma-CVD method which used SiF4 and N2 for the raw material, or SiF4 and N2O is made into material gas, and nitriding oxidation silicon film or these cascade screens are formed.
[0034] Moreover, it heat-treats within the limits of 300-450 degrees C after surface protective coat 13 formation in inert gas, oxygen, or these mixed-gas ambient atmospheres.
[0035] Although the PZT film was used as ferroelectric film with the gestalt of the above-mentioned implementation, it is also possible for this invention not to be limited to this and to use a bismuth stratified compound (SrBi4Ti 4O15, SrBi2Ta 2O9).
[0036]
[Effect of the Invention] As mentioned above, without degrading a ferroelectric property by using this invention, as explained to the detail, termination of the defect of the interface of the gate oxide of a switching transistor and a silicon substrate is carried out by hydrogen, the interface-state-density consistency of gate oxide is reduced, and stable transistor characteristics are acquired.

[0037] Moreover, by using the interlayer insulation film and surface protective coat which do not contain hydrogen, since hydrogen dissociation by heat treatment does not arise, degradation of a ferroelectric property is not seen. Moreover, since the above-mentioned heat treatment temperature was made into 300-450 degrees C, the reaction of the aluminum at the time of using aluminum for wiring and a silicon substrate can be controlled, and the dependability of aluminum wiring can be secured.
[0038] Furthermore, heat treatment after surface protective coat formation recovers opening of a contact hole, processing of metal wiring, and the plasma damage introduced into a surface protective coat formation process. Moreover, the hydrogen which carried out termination of the defect of the gate oxide-substrate interface of a transistor is stable within the limits of 300-450 degrees C, without dissociating.
[0039] Therefore, compared with the conventional approach, the semi-conductor storage element which has good transistor characteristics and a ferroelectric property and which can be operated stably can be manufactured.

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CLAIMS

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[Claim(s)]
[Claim 1] The MOS transistor used as the switching transistor formed in the semi-conductor substrate, Connect with the above-mentioned MOS transistor and an electric target through the contact hole formed in the 1st interlayer insulation film, have the capacitor which makes the ferroelectric film a dielectric film, and wiring is minded. In the manufacture approach of the semi-conductor storage element connected with other semi-conductor storage elements By carrying out 1st heat treatment in the mixed ambient atmosphere of hydrogen or hydrogen, and inert gas, after crystallizing the above-mentioned ferroelectric film, the process which forms the above-mentioned ferroelectric film on the lower electrode of the above-mentioned capacitor, and The process which carries out termination of the defect in the interface of the gate dielectric film of the above-mentioned MOS transistor, and the above-mentioned semi-conductor substrate, The process which forms the up electrode of the above-mentioned capacitor through the contact hole formed in direct or the 2nd interlayer insulation film on the above-mentioned ferroelectric film, The manufacture approach of the semi-conductor storage element characterized by forming a contact hole, forming wiring which connects the above-mentioned MOS transistor and other semi-conductor storage elements, and forming a surface protective coat in a front face after that after forming the 3rd interlayer insulation film.
[Claim 2] The manufacture approach of the semi-conductor storage element according to claim 1 characterized by performing the 1st above-mentioned heat treatment at 300-450 degrees C.
[Claim 3] The manufacture approach of the semi-conductor storage element according to claim 1 or 2 characterized by forming the oxidation silicon film, silicon nitride film, or nitriding oxidation silicon film containing a fluorine by the chemical vapor deposition which used silicon tetrafluoride as a raw material as the 1st interlayer insulation film of the above, the 2nd interlayer insulation film of the above, the 3rd interlayer insulation film of the above, and the above-mentioned surface protective coat.
[Claim 4] The manufacture approach of the semi-conductor storage element according to claim 1 to 3 characterized by carrying out 2nd heat treatment in the mixed-gas ambient atmosphere of oxygen, inert gas, or oxygen and inert gas after forming the above-mentioned surface protective coat.
[Claim 5] The manufacture approach of the semi-conductor storage element according to claim 1 to 4 characterized by performing the 2nd above-mentioned heat treatment at 300-450 degrees C.

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* NOTICES *



1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

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DRAWINGS

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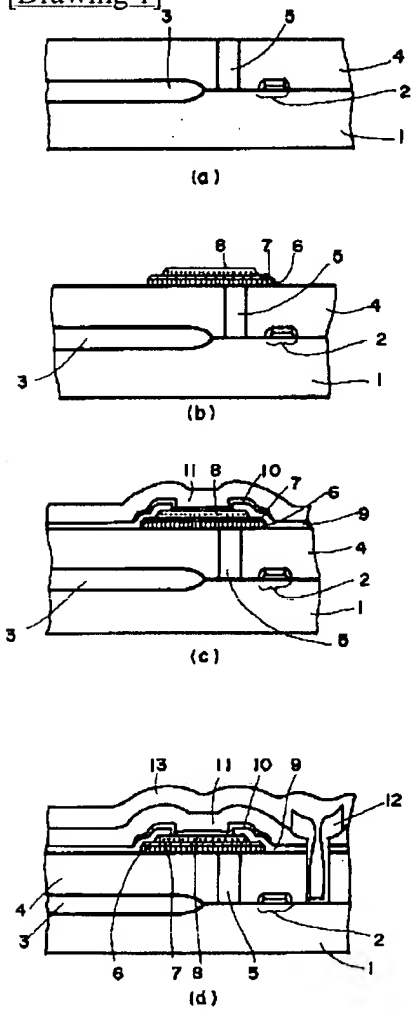
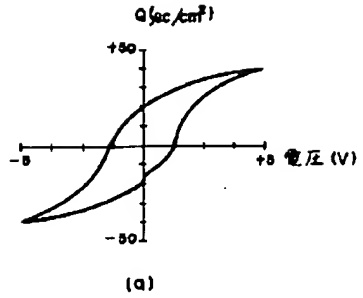
[Drawing 1]




[Drawing 2]

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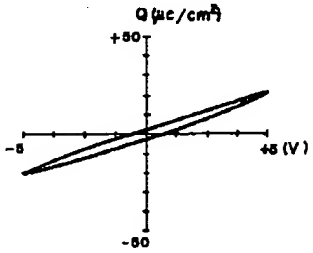
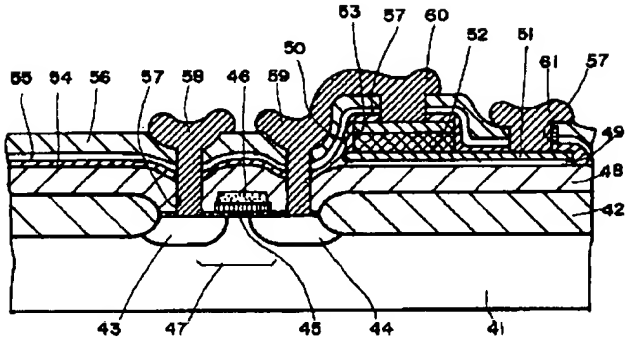



(b)

[Drawing 3]

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